Tentative EE 330 Daily Coverage and Reading Materials - Fall 2019

Suggested Reading Materials are listed on a weeklly basis. Chapter references are to the Weste Harris test. See Table of Contents for specific sections.

			Period	Topics (exam dates not shown)
Week	25-Aug	1		Chapter 1, Notes
			1	Electronic systems overview, economic opportunities
			2	Design approaches,yield and cost of semiconductor products
			3	Physical characteristics, soft faults
Week	1-Sep	2		Chapter 1, Notes
				Holiday
			4	Digital systems - basic gates, switch-level MOS models
			5	Digital systems - complex logic gates, pass transistor logic, Improved switch-Level MOS model
Week	8-Sep	3		Chapter 1, Notes
			6	Paramater extraction for Imp. switch-level model, propagation delay in logic, placement, stick diagrams
			7	Technology files, design rules, layout
			8	Fabrication technology, processing steps
Week	15-Sep	4		Chapter 1 Chapter 3, Chapter 6, Notes
			9	Fabrication technology, processing steps
			10	Interconnects - resistive and capacitive
			11	Back-end technology ; packaging, bonding, basic semiconductorpProcesses
Week	22-Sep	5		Chapter 2 Chapter 6, Notes
			12	Devices/Device Models in semiconductor proceses - resistors, diodes
			13	Diode operation, diode model (diode equation), simplified diode models
			14	Exam 1
Week	29-Sep	6		Chapter 2, Chapter 3, Notes
			15	Diode applications, capacitor types and models, MOSFET operation
			16	MOSFET Operation - square law model, short channel model, BSIM model (brief)
			17	MOS process description - (n-channel, p-channel, capacitors, resistors)
Week	6-Oct	7		Notes
			18	Small feature MOS processes, bipolar devices, operation, device models
			19	Bipolar process description - (vertical and lateral devices, JFET, diffused resistor, varactor, diode)
			20	Bipolar devices - JFET and Thyristors
Week	13-Oct	8		Notes
			21	Bipolar devices - JFET and Thyristors
			22	Thyristors
			23	Amplification in transistor circuis
Week	20-Oct	9		Notes
			24	Amplification in transistor circuits
			25	Small-signal principles, ss equivalent circuits, ss diode model
			26	Exam 2
Week	27-Oct	10		Notes
			27	Small-signal models of n-terminal devices, MOSFET and BJT ss models
			28	Application of ss models, graphical analysis of nonlinear transistor circuits,comparison of MOS and BJT amplifiers
			29	Basic amplifier structures-CS/CE, CD/CC, CG/CB
Week	3-Nov	11		Notes
			30	High gain amplifiers - cascoding, cascading
			31	Current source biasing, darlington configuration
			32	Current sources and mirrors
Week	10-Nov	12		Chapter 9, Notes
			33	Differential amplifiers (brief), bipolar and MOS mappings
			34	Heirarchiacal digital design - behavioral, structural, physical, digital design flows
			35	Basic gates, charatristics of logic families
Week	17-Nov	13		Chapter 9, Notes
			36	Inverter pair, analysis of CMOS inverter
			37	Other CMOS logic circuits, static power dissipation, propatagion delay
			38	Exam 3
Week	1-Dec	14		Chapter 4, Notes
			39	The Reference Inverter, sizing of gates
			40	Propagation delay in multiple levels of logic, asymetric overdrive, optimally driving large capacitive loads
			41	Optimally driving large capacitive loads
Week	8-Dec	15		Chapter 4, Notes
			42	Logic effort, Elmore delay, power dissipation in logic circuits
			43	Sequential logic - latches, flip flops, shift registers, array logic, memory structures
			44	High frequency MOS model